CURRICULUM VITAE (D.Sc. (Tech.) Tero Säntti, 31.01.2022)

Name:	**Tero** Antti Mikael **Säntti**
Date of Birth:	18 April 1974
Place of Birth:	Finland
Nationality:	Finnish
Languages:	Finnish, English, Swedish, (German, Japanese)
Marital Status:	Common-law marriage

Academic Degrees: *D.Sc. (Tech.)* in Microelectronics (Computer Systems), University of Turku, Finland, 2008
M.Sc. in Electronics and Information Technology, University of Turku, Finland, 2002.

Current Positions: Senior Research Fellow, University of Turku, Finland (1/2017 ->)

Senior Engineer, Aboa Space Research Oy (ASRO), Finland, (5/2011 ->), co-owner (3/2013 ->), Chairman of the Board (5/2021 ->)

Senior Engineer, Kovilta Oy, Finland, (6/2017 ->)

Previous Positions: Senior Research Fellow / Erikoistutkija, Technology Research Center, Brahea Centre, University of Turku
Senior Researcher / Erikoistutkija, Business and Innovation Development (BID Technology), University of Turku
Senior Researcher / Erikoistutkija (Embedded Computer Systems), Department of Information Technology, University of Turku
Researcher / Tutkija (Computer Systems), Department of Information Technology, University of Turku
Assistant / Assistentti (Digital and Computer Technology), Department of Information Technology, University of Turku
Lecturer / Lehtori (Digital and Computer Technology), Department of Information Technology, University of Turku
Researcher / Tutkija (Digital and Computer Technology), Department of Information Technology, University of Turku
Researcher / Tutkija (SoC-Mobinet EU project), Department of Information Technology, University of Turku
Assistant / Assistentti, Department of Applied Physics, University of Turku
Research associate / Tutkimusavustaja, Department of Applied Physics, University of Turku

Other Employments: On commission, Aboa Space Research Oy (ASRO), Finland, design and implementation of a FPGA prototype and related control software for a satellite instrument (6/2009 – 12/2009),
On commission, Aboa Space Research Oy (ASRO), Finland, electronics and PCB design and testing (9/2005 – 12/2005),
On commission, Minima Processor Oy, Finland, FPGA design

Miscellaneous short term employments since 1989, including postal services, security guard, land-measurement, catalogue publication and others.

Research Activities: Since 1998 Säntti has been interested in electronic circuit design, embedded systems and system level integration. In the beginning his focus was on implementation of high speed asynchronous wave-pipelined arithmetic units, on which he wrote his M.Sc. thesis. During the next 8 years he was focusing on Java Virtual Machine architecture development based on a novel Java accelerator core. The emphasis was on improved real time performance and predictability with low power usage. This was the topic of his D.Sc. (Tech.) thesis. He is also interested in FPGA prototyping and microprocessor based multicore systems, and most recently in dynamic (runtime) reconfiguration of such systems. Especially aerospace applications and fault tolerance in FPGAs are high on his list of interests. Besides his core interests he is also involved in embedded software design and implementing embedded operating systems, mainly Linux running on various FPGA platforms and embedded processors. Visual data processing and content analysis are high on his list of interests, as well as the application of such systems to real life problems. Besides 3D localization, the applications have ranged from extracting space debris from optical images to monitoring and controlling of high power laser welding. These far ends represent the polar opposites in terms of speed, several seconds of exposure time for the debris vs. 1000 fps for welding, and also in processing capability, high performance computers for debris vs. embedded system for welding.

Publications: The D.Sc. (Tech.) thesis of Säntti was "A Co-Processor Approach for Efficient Java Execution in Embedded Systems", University of Turku, 2008.
Säntti has published 72 publications (According to Google Scholar). Additionally he has authored numerous documents on the FPGA development for the ESA/Solar Orbiter/EPD/LET project, on the ESA/ISOOS project, on the ESA/StreakDet project and on the ESA/EuCPAD project. Five selected publications:

[1] T. Säntti, J. Tyystjärvi and J. Plosila, "Java Co-Processor for Embedded Systems", in Processor Design - System-On-Chip Computing for ASICs and FPGAs. Nurmi, Jari, editor, chapter 13, pages 287-308. Springer, 2007
[2] B. Yang, L. Guang, T. Säntti and J. Plosila, "Mapping Multiple Applications with Unbounded and Bounded Number of Cores on Many-Core Networks-on-Chip", In Microprocessors and Microsystems, Elsevier, 2012
[3] J. Tyystjärvi, T. Säntti and J. Plosila, "Efficient Execution of Switch Instructions on a Multicore Java Co-Processor System", in Proc. TechPos 2009, Kuala Lumpur, Malaysia, 2009, *Won the Best Paper Award*
[4] T. Säntti, J. Poikonen, O. Lahdenoja, M. Laiho, A. Paasio, "Online seam tracking for laser welding with a vision chip and FPGA enabled camera system", In Proc. ISCAS 2015, Lisbon, Portugal, 2015
[5] T. Säntti, O. Lahdenoja, A. Paasio, M. Laiho, J. Poikonen, "Line Detection on FPGA with parallel sensor-level segmentation", In Proc. Cellular Nanoscale Networks and their Applications (CNNA), Notre Dame, USA, 2014