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Hashem Haghbayan

Curriculum Vitae

Research Interest

Autonomous systems, Computing systems, Machine-learning, Robot control systems, Battery modeling and management.

Positions

Current	Adjunct professor (Docent), **University of Turku**, Turku, Finland
October 2023	Senior Research Fellow, **University of Turku**, Turku, Finland
September 2023	Adjunct professor (Docent), **University of Turku**, Turku, Finland
April 2022	Postdoc researcher, **University of Turku**, Turku, Finland
March 2022	Postdoc researcher, **University of Turku**, Turku, Finland
July 2021	Advisors: Prof. Juha Plosila and Prof. Jukka Heikkonen
	Visiting researcher, **Plitecnico di Milano**, Milan, Advisor: Prof. Antonio Miele
June 2021	Visiting researcher, **SAFARI** research group, **ETH Zürich**, Zürich
Jan 2021	Advisors: Prof. Onur Mutlu
Dec 2020	Postdoc researcher, **University of Turku**, Turku, Finland
Jan 2018	Advisors: Prof. Juha Plosila and Prof. Jukka Heikkonen
Dec 2017	Doctoral degree in Computer Architecture, **University of Turku**, Turku, Finland
Sep 2013	Thesis: "Energy-Efficient and Reliable Computing in Dark Silicon Era"
	Advisors: Prof. Hannu Tenhunen and Prof. Pasi Liljeberg
Apr 2013	Circuit designer and FPGA developer at Sinamicro
Sep 2012	Advisor: Prof. Mehdi Fakhraie
Sep 2012	Verilog-based designer and FPGA developer, **University of Tehran**, Tehran, Iran.
Nov 2009	Advisors: Prof. Mehdi Fakhraie and Prof. Zainalabedin Navabi
	I designed a low power ASIC processor with DSP custom instructions for a wireless sensor network
Sep 2009	Master Degree in Computer engineering, **University of Tehran**, Tehran, ,Iran.
Oct 2006	Thesis: "Transaction Level Concurrent BIST in SoCs" | Advisor: Prof. Zainalabedin Navabi
Sep 2006	Bachelor's Degree in Computer engineering, **Ferdowsi University of Mashhad**, Mashhad, ,Iran.
Oct 2001	Thesis: "Exploring Ships Dynamic and Handling Using MATLAB & SIMULINK (from control perspective)"
	Advisor: Prof. Ghodrat Sepidnam

Awards and Honors

2021 Nokia Jorma Ollila grant to visit **Plitecnico di Milano**
2021 Best paper nomination at 35th ECMS International Conference on Modelling and Simulation (ECMS), Germany
2020 Nokia Jorma Ollila grant to visit **Plitecnico di Milano**
2020 HiPEAC EU research collaboration grant to visit **ETH Zürich**
2020 Best paper nomination at ACM/IEEE Design Automation and Test in Europe (DATE) Conference, France.
2019 Best paper award at ACM International Symposium on Computer Science and Intelligent Control (ISCSIC 2019), Netherlands
2018 Honored Doctoral Degree: evaluated by the reviewers to be in the top 10% internationally
2016 Nokia Foundation Research Excellence Award
2015 Nokia Foundation Research Excellence Award.
2015 Best paper nomination at IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2015
2014 4-year fellowship for Doctoral Degree from University of Turku Graduate School (UTUGS)

Completed projects

Tool Development	Developing a tool for camera calibration based on LiDAR and GPS data for an autonomous boat system Integrating dynamic voltage-frequency scaling (DVFS), cache partitioning, MCPAT, Lumos, PIN trace of PARSEC benchmarks, data analysis patch (with **Python**), and HotSpot with Noculator (a shared memory many-core simulator developed in **C#**). Also integrating DVFS, MCPAT, Lumos, Run-time mapping, and Hotspot to Noxim (a message-passing many-core simulator with **SystemC**) Developing a tool, i.e., NetlistGen, with **C++** to add test features automatically to Verilog RTL codes. Developing a tool, i.e., STG, in **C++**, for fast generation of high quality test patterns for testing the sequential circuits.
Industrial Projects	Designing a controller, in MATLAB environment, for hydraulic valves of an autonomous arm robot 5-stage pipeline processor based on SPARC ISA with **Verilog** HDL and emulated it on Altera FPGA. Floating point, dependency, and forwarding is supported. $CPI \approx 1.5$. A low power ASIC processor with DSP custom instructions for a wireless sensor network SoC with **Verilog** HDL and emulating it on Xilinx FPGA. The chip fabricated in 135nm technology. The controller of a 5-stage pipeline processor with **VHDL** and emulating it on Xilinx FPGA.

Patent

Iran Patent	**M.H. Haghbayan**, with A. Mazraie, M.S. Jahangiri, A. Yazdanbakhsh, H. Dorosti, M.E. Salehi, and S.M. Fakhraie,„ "Architecture Specifications of Wireless Sensor Network Processor of the University of Tehran (Light Processor)," in Iran patent, NO. 139250840003000105, Year 2013.

Publications

After PhD (Journals)

1. **IEEE TC**: **H. Haghbayan**, A. Miele, O. Mutlu, J. Plosila, "Run-time Resource Management in CMPs Handling Multiple Aging Mechanisms," in IEEE Transactions on Computers, 2023.
2. **IEEE-Access**: M. Rabah, **H. Haghbayan**, E. Immonen, J. Plosila, "An AI-in-Loop Fuzzy-Control Technique for UAV's Stabilization and Landing," IEEE Access, 2022.
3. **Sensors**: H. Mahboob, J.N. Yasin, S. Jokinen, **M.H. Haghbayan**, J. Plosila, M.M. Yasin, "DCP-SLAM: Distributed Collaborative Partial Swarm SLAM for Efficient Navigation of Autonomous Robots, " Sensors 23(2), 2023.
4. **IEEE-Access**: A. Tahir, **H. Haghbayan**, J. Böling, J. Plosila, "Energy-efficient Post-failure Reconfiguration of Swarms of Unmanned Aerial Vehicles," IEEE Access, 2022.

5. **JIDPS:** S. Shahsavari, M. Rabah, E. Immonen, **M-H. Haghbayan**, J. Plosila, "Remote Run-Time Failure Detection and Recovery Control For Quadcopters," Journal of Integrated Design and Process Science, vol. Pre-press, no. Pre-press, pp. 1-21, 2021.
6. **MDPI**: J. Yasin, H. Mahboob, **M-H. Haghbayan**, M. Yasin, J. Plosila, "Energy-Efficient Navigation of an Autonomous Swarm with Adaptive Consciousness," Remote. Sens. 13(6): 1059, 2021.
7. **Elsevier-Heliyon**: J.N. Yasin, **M-H. Haghbayan**, M. Yasin, J. Plosila, "Swarm Formation Morphing for Congestion-Aware Collision Avoidance," Elsevier Heliyon, 2021.
8. **IEEE-Access**: M. Rabah, A. Rohan, **M-H. Haghbayan**, J. Plosila, S. Kim, "Heterogeneous Parallelization for Object Detection and Tracking in UAVs," IEEE Access, 2020.
9. **IEEE-Access**: J. Yasin, S. Mohamed, **M-H. Haghbayan**, J. Heikkonen, H. Tenhunen, J. Plosila, "Unmanned Aerial Vehicles (UAVs): Collision Avoidance Systems and Approaches," IEEE Access, 2020.
10. **IEEE-Access**: J. Yasin, S. Mohamed, **M-H. Haghbayan**, J. Heikkonen, H. Tenhunen, J. Plosila, "Energy-efficient Formation Morphing for Collision Avoidance in a Swarm of Drones," IEEE Access, 2020.
11. **IEEE-Access**: A. Tahir, J. Böling, **M-H. Haghbayan**, J. Plosila, "Comparison of Linear and Nonlinear Methods for Distributed Control of a Hierarchical Formation of UAVs," IEEE Access, 2020.
12. **IEEE-Access**: S. Mohamed, **M-H. Haghbayan**, J. Heikkonen, H. Tenhunen, J. Plosila, "A Survey on Odometry for Autonomous Navigation Systems," IEEE Access, 2019.
13. **Elsevier-NTEGRATION**: A. Tahir, J. Böling, **M-H. Haghbayan**, H. Toivonen, J. Plosila, "Swarms of Unmanned Aerial Vehicles – A Survey," Journal of Industrial Information Integration, 2018.
14. **IEEE TC**: A. Kanduri, **M.H. Haghbayan**, A.M. Rahmani, M. Shafique, A. Jantsch, P. Liljeberg, "adBoost: Thermal Aware Performance Boosting through Dark Silicon Patterning," IEEE Transactions on Computers, 2018.
15. **IEEE TVLSI**: Anil Kanduri, **M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, A. Jantsch, H. Tenhunen, N. Dutt, "Accuracy Aware Power Management for Many-core Systems running Error Resilient Applications," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017.
16. **IEEE TC**: **M.H. Haghbayan**, A. Miele, A.M. Rahmani, P. Liljeberg, H. Tenhunen, "Performance/Reliability-aware Resource Management for Many-Cores in Dark Silicon Era," in IEEE Transactions on Computers, 2017.
17. **IEEE D&T**: **M.H. Haghbayan**, A. Miele, A.M. Rahmani, P. Liljeberg, A. Jantsch, C. Bolchini, H. Tenhunen, "Can Dark Silicon Be Exploited to Prolong System Lifetime?," in IEEE Design and Test of Computers, 2017.
18. **IEEE TVLSI**: A.M. Rahmani, **M.H. Haghbayan**, A. Miele, P. Liljeberg, A. Jantsch, H. Tenhunen, "Reliability-Aware Runtime Power Management for Many-Core Systems in the Dark Silicon Era," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017.
19. **IEEE TC**: **M.H. Haghbayan**, A.M. Rahmani, A. Miele, M. Fattah, J. Plosila, P. Liljeberg, H. Tenhunen, "A Power-Aware Approach for Online Test Scheduling in Many-core Architectures," in IEEE Transactions on Computers, 2016.

(Conferences)

1. **ECMS 2023**: M. Heydarzadeh, E. Immonen, H. Haghbayan, J. Plosila, "A Light-weight Model for Run-time Battery SOC-SOH Estimation While Considering Aging, " The 37th ECMS International Conference on Modelling and Simulation (ECMS), Norway, 2022.
2. **ISIE 2023**: M. Karami, S. Shahsavari, E. Immonen, H. Haghbayan, J. Plosila, "An Extension of the Kinetic Battery Model for Optimal Control Applications," 32nd International Symposium on Industrial Electronics (ISIE), Finland 2023
3. **DATE 2023**: M. Karami, E. Immonen, S. Shahsavari, **H. Haghbayan**, J. Plosila, "A Coupled Battery State-of-Charge and Voltage Model for Optimal Control Applications", in IEEE/ACM Design, Automation, and Test in Europe (DATE), Belgium, 2023.
4. **DFT 2022**: M. Karami, **H. Haghbayan**, M. Ebrahimi, A. Miele, J. Plosila, "Thread-level Parallelism in Fault Simulation of Deep Neural Networks on Multi-Processor Systems", in IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2022), USA.
5. **PAAMS 2022**: J. Yasin, H. Mahboob, S. Jokinen, **H. Haghbayan**, M-M. Yasin, Juha Plosila, "Partial Swarm SLAM for Intelligent Navigation," in 20th International Conference on Practical Applications of Agents and Multi-Agent Systems, 2020, Italy.
6. **ECMS 2022**: S. Shahsavari, E. Immonen, M. Rabah, M-H. Haghbayan, J. Plosila, "How to run a world record? A Reinforcement Learning approach, " The 36th ECMS International Conference on Modelling and Simulation (ECMS), Norway, 2022.
7. **IROS 2021**: S. Mohamed, **M.H. Haghbayan**, A. Miele, O. Mutlu, J. Plosila, "Energy-Efficient Mobile Robot Control via Run-time Monitoring of Environmental Complexity and Computing Workload," The IEEE/RSJ International Conference on Intelligent Robots and Systems(IROS), Czech 2021.
8. **ECMS 2021**: S. Shahsavari, E. Immonen, M. Rabah, M-H. Haghbayan, J. Plosila, "MCX ? An Open-Source Framework For Digital Twins, " The 35th ECMS International Conference on Modelling and Simulation (ECMS), Germany, 2021. **Nominated for best paper award**

9. **ECMS 2021**: M. Rabah, E. Immonen, S. Shahsavari, M.H... Haghbayan, K. Murashko, J. Plosila, "Capacity Loss Estimation For Li-Ion Batteries Based On A Semi-Empirical Model, " The 35th ECMS International Conference on Modelling and Simulation (ECMS), Germany, 2021.
10. **PDP 2021**: Masoomeh Karami, Mohammad-Hashem Haghbayan, Masoumeh Ebrahimi, Hamid Nejatollahi, Hannu Tenhunen, Juha Plosila, "High-Performance Parallel Fault Simulation for Multi-Core Systems, " The European International Conference on Parallel, Distributed, and Network-Based Processing, Spain, 2021.
11. **ETS 2021**: M. Karami, **M.H. Haghbayan**, M. Ebrahimi, A. Miele, H. Tenhunen, J. Plosila, "Hierarchical Fault Simulation of Deep Neural Networks on Multi-Core Systems", in IEEE European Test Symposium (ETS), 2021, Belgium.
12. **FICC 2021**: J. Yasin, S. Mohamed, **M.H. Haghbayan**, J. Heikkonen, H. Tenhunen, Juha Plosila, "Dynamic Formation Reshaping Based on Point Set Registration in a Swarm of Drones," in IEEE, Future of Information and Communication Conference, 2021, Canada.
13. **DATE 2020**: **M.H. Haghbayan**, A. Miele, H. Tenhunen, Juha Plosila, "Thermal-Cycling-aware Dynamic Reliability Management in Many-Core System-on-Chip," in IEEE/ACM Design, Automation, and Test in Europe, 2020, France. **Nominated for best paper award**
14. **ISVC 2020**: J. Yasin, S. Mohamed, **M.H. Haghbayan**, J. Heikkonen, H. Tenhunen, Juha Plosila, "Asynchronous Corner Tracking Algorithm based on Lifetime of Events for DAVIS Cameras," in IEEE, 15th International Symposium on Visual Computing, 2020, USA.
15. **PAAMS 2020**: J. Yasin, S. Mohamed, **M.H. Haghbayan**, J. Heikkonen, H. Tenhunen, Juha Plosila, "Navigation of Autonomous Swarm of Drones using Translational Coordinates," in 18th International Conference on Practical Applications of Agents and Multi-Agent Systems, 2020, Italy.
16. **ICPR 2020**: S. Mohamed, J. Yasin, **M.H. Haghbayan**, J. Heikkonen, H. Tenhunen, Juha Plosila, "Dynamic Resource-Aware Corner Detection for Bio-Inspired Vision Sensors," in International Conference on Pattern Recognition (ICPR'2020), 2020, Italy.
17. **ECMS 2020**: A. Tahir, J. Böling, **M.H. Haghbayan**, J. Plosila, "Navigation System For Landing A Swarm Of Autonomous Drones On A Movable Surface," 34th International ECMS Conference on Modeling and Simulation, Germany 2020.
18. **AICV 2020**: S. Mohamed, **M.H. Haghbayan**, J. Heikkonen, H. Tenhunen, Juha Plosila, "Towards Real-time Edge Detection for Event Cameras Based on Lifetime and Dynamic Slicing," in International Conference on Artificial Intelligence and Computer Vision (AICV'2020), 2020, Egypt.
19. **INTSYS 2019**: S. Mohamed, **M.H. Haghbayan**, J. Heikkonen, H. Tenhunen, J. Plosila, "Towards Dynamic Monocular Visual Odometry Based on an Event Camera and IMU Sensor," International Conference on Intelligent Transport Systems (INTSYS 2019), Portugal 2019.
20. **ISCSIC 2019**: J. Yasin, **M.H. Haghbayan**, J. Heikkonen, H. Tenhunen, J. Plosila, "Formation/Collision Co-awareness in a Swarm of Drones," 3th International Symposium on Computer Science and Intelligent Control (ISCSIC 2019), Netherlands 2019. **Best paper award**
21. **ICMV 2019**: S. Mohamed, **M.H. Haghbayan**, J. Heikkonen, H. Tenhunen, J. Plosila, "Moncoular Visual Odometry Based on Hybrid Parameterization," 12th International Conference on Machine Vision (ICMV 2019), Netherlands 2019.
22. **ICMLA 2018**: F. Farahnakian, **M.H. Haghbayan**, J-K. Poikonen, M. Laurinen, P. Nevalainen, J. Heikkonen, "Object Detection based on Multi-sensor Proposal Fusion in Maritime Environment," IEEE International Conference on Machine Learning and Applications(ICMLA), 2018, USA.
23. **ITSC 2018**: **M.H. Haghbayan**, F. Farahnakian, J-K. Poikonen, M. Laurinen, P. Nevalainen, J. Plosila, J. Heikkonen, "An Efficient Multi-sensor Fusion Approach for Object Detection in Maritime Environments," IEEE International Conference on Intelligent Transportation Systems (ITSC), 2018, USA.
24. **ISCAS 2018**: A. Kanduri, **M.H. Haghbayan**, A-M. Rahmani, P. Liljeberg, "Approximation for Runtime Power Management," IEEE International Symposium on Circuits and Systems (ISCAS), 2018, Italy.
25. E. Sadredini, **M.H. Haghbayan**, M. Fathy, Z. Navabi, "Test Generation and Scheduling for a Hybrid BIST Considering Test Time and Power Constraint," in Distributed Parallel and Cluster Computing, 2017.
26. **DATE 2016**: **M.H. Haghbayan**, A. Miele, A.M. Rahmani, P. Liljeberg, H. Tenhunen, "A Lifetime-Aware Runtime Mapping Approach for Many-core Systems in the Dark Silicon Era," in IEEE/ACM Design, Automation, and Test in Europe, 2016, Germany.
27. **ICCAD 2016**: A. Kanduri, **M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, A. Jantsch, N. Dutt, H. Tenhunen, "Approximation Knob: Power Capping Meets Energy Efficiency," in IEEE/ACM International Conference on Computer-Aided Design (ICCAD'16), 2016, USA.

28. **ICPRAM 2016** P. Nevalainen, **M.H. Haghbayan**, A. Kauhanen, J. Pohjankukka, M. Laakso, J. Heikkonen, "Real-Time Swimmer Tracking on Sparse Camera Array" Pattern Recognition: Applications and Methods, 5th International Conference, ICPRAM 2016, France, Febryary 24-27. Revised Selected Papers , 2017.
29. **ICCD 2015**: A. Kanduri, **M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, A. Jantsch, H. Tenhunen, "Dark Silicon Aware Runtime Mapping for Many-core Systems: A Patterning Approach," in IEEE/ACM International Conference on Computer Design, 2015, USA.
30. **DFT 2015**: **M.H. Haghbayan**, S. Teravainen, A.M. Rahmani, P. Liljeberg, H. Tenhunen, "Adaptive Fault Simulation on Many-core Microprocessor Systems," in IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2015), USA.
31. **DFT 2015**: S. Teravainen, **M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, H. Tenhunen, "Software-Based On-Chip Thermal Sensor Calibration for DVFS-enabled Many-core Systems," in IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT 2015), USA. **Nominated for best paper award**
32. **NOCS 2015**: **M.H. Haghbayan**, A. Kanduri, A.M. Rahmani, P. Liljeberg, A. Jantsch, H. Tenhunen, "MapPro: Proactive Runtime Mapping for Dynamic Workloads by Quantifying Ripple Effect of Applications on Networks-on-Chip," in IEEE/ACM International Symposium on Networks-on-Chip (NOCS'15), 2015, Canada.
33. **ISLPED 2015**: A.M. Rahmani, **M.H. Haghbayan**, A. Kanduri, A. Yemane, P. Liljeberg, J. Plosila, A. Jantsch, H. Tenhunen, "Dynamic Power Management for Many-Core Platforms in the Dark Silicon Era: A Multi-Objective Control Approach," in IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED'15), 2015, Italy.
34. **MCSoC 2015** E. Karimi, **M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, Z. Navabi, "Accelerated On-Chip Communication Test Methodology Using a Novel High-Level Fault Model," in Proc. of the IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip, 2015, 2015, Italy.
35. **DATE 2015**: **M.H. Haghbayan**, A.M. Rahmani, M. Fattah, P. Liljeberg, J. Plosila, Z. Navabi, H. Tenhunen, "Power-Aware Online Testing of Manycore Systems in the Dark Silicon Era," in IEEE/ACM the Design, Automation, and Test in Europe (DATE), 2015, France.
36. **ICCD 2014**: **M.H. Haghbayan**, A.M. Rahmani, A. Yemane, P. Liljeberg, J. Plosila, A. Jantsch, H. Tenhunen, "Dark Silicon Aware Power Management for Manycore Systems under Dynamic Workloads," in IEEE/ACM The 32nd IEEE/ACM International Conference on Computer Design (ICCD 2014), Korea.
37. **DFT 2014**: **M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, J. Plosila, H. Tenhunen, "Energy-Efficient Concurrent Testing Approach for Many-Core Systems in the Dark Silicon Age," in IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems DFT 2014, Netherlands.
38. **MEDIAN-DFT 2014 M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, J. Plosila, H. Tenhunen, "Distributed BIST Approach for Power Constrained Many-Core Systems," in Proc. of Joint MEDIAN–TRUDEVICE Open Forum Co-Located with IEEE 17th International Symposium on Design and Diagnostics of Electronic Circuits Systems, 2014, Netherlands.
39. **DFT 2014**: **M.H. Haghbayan**, B. Alizadeh, A.M. Rahmani, P. Liljeberg, H. Tenhunen, "Automated Formal Approach for Debugging Dividers Using Dynamic Specification," in IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems DFT 2014, Netherlands.
40. **DDECS 2014**: **M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, J. Plosila, H. Tenhunen, "Online Testing of Many-Core Systems in the Dark Silicon Era," in IEEE Design and Diagnostics of Electronic Circuits & Systems, 2014, Poland.
41. **EWDTS 2014** V. Janfaza, P. Foroutan, B. Forouzandeh, **M.H. Haghbayan**, " A mathematical model for estimating acceptable ratio of test patterns," in IEEE East-West Design & Test Symposium, 2014, Russia.
42. **VLSID 2014 M.H. Haghbayan**, Bijan Alizadeh, Payman Behnam, Saeed Safari, "Formal Verification and Debugging of Array Dividers With Auto-Correction Mechanism," in Proc. of 27th IEEE International Conference on VLSI Design 2014, Bombay, India.
43. **VLSI-SoC 2013** E. Karimi, **M.H. Haghbayan**, A. Maleki, M. Tabande "Graph Based Fault Model Definition for Bus Testing," in Proc. of the 21st IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) ., 2013, Turkey.
44. **EWDTS 2013** S. Hoseinzadeh, **M.H. Haghbayan**, "High-level test program generation strategies for processors," in IEEE East-West Design & Test Symposium, 2013, Russia.
45. **EWDTS 2013** E. Karimi, A. Maleki, **M.H. Haghbayan**, M. Tabandeh, "Functional fault model definition for bus testing," in IEEE East-West Design & Test Symposium, 2013, Russia.
46. **EWDTS 2013** E. Karimi, M. Tabandeh, **M.H. Haghbayan**, "Test data compression strategy while using hybrid-BIST methodology," in IEEE East-West Design & Test Symposium, 2013, Russia.
47. **DDECS 2012 M.H. Haghbayan**, S. Safari, Z. Navabi "Power Constraint Testing for Multi-Clock Domain SoCs Using Concurrent Hybrid BIST," in Proc. of the IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits Systems., 2012, Estonia.

48. **ATS 2011**: B. Khodabandeloo, S.A. Hoseini, S. Taheri, **M.H. Haghbayan**, M.R. Babaei, Z. Navabi, "Online Test Macro Scheduling and Assignment in MPSoC Design," in IEEE Asian Test Symposium, 2011, India.
49. **ATS 2010**: **M.H. Haghbayan**, F. Javaheri, S. Karamati, Z. Navabi, "Test Pattern Selection and Compaction for Sequential Circuits in an HDL Environment," in IEEE Asian Test Symposium, 2010, China.
50. **EWDTS 2010**: **M.H. Haghbayan**, Z. Navabi, "Architecture design and technical methodology for bus testing," in IEEE East-West Design & Test Symposium, 2010, Russia.
51. **EWDTS 2010**: **M.H. Haghbayan**, A. Yazdanpanah, S. Karamati, R. Saeedi, Z. Navabi, "Generating test patterns for sequential circuits using random patterns by PLI functions," in IEEE East-West Design & Test Symposium, 2010, Russia.
52. **WRTLT 2009** N. Nemati, A. Kamran , M.H. Sargolzaie, **M.H. Haghbayan**, Z. Navabi, "An Optimal HDL-based Approach for Mixed-level Hierarchical Fault Simulation," in Proc. of the IEEE Workshop on RTL and High Level Testing., 2010, India.
53. **WRTLT 2008** M.H. Sargolzaie, **M.H. Haghbayan**, S. Safari "RTL Concurrent Error Detection using Modular Partitioning Technique," in Proc. of the IEEE Workshop on RTL and High Level Testing., 2008, Japan.

Book Chapters

Springer 2016	**M.H. Haghbayan**, A.M. Rahmani, A. Miele, P. Liljeberg, and H. Tenhunen, "Online Software-Based Self-Testing in the Dark Silicon Era", *in The Dark Side of Silicon (Computing in the Dark Silicon Era), Springer, 2016*.
Springer 2016	A.M. Rahmani, **M.H. Haghbayan**, P. Liljeberg, A. Jantsch, and H. Tenhunen, "A Multi-Objective Power Management for CMPs in the Dark Silicon Age", *in The Dark Side of Silicon (Computing in the Dark Silicon Era), Springer, 2016*.
Springer 2016	A. Kanduri, **M.H. Haghbayan**, A.M. Rahmani, P. Liljeberg, A. Jantsch, and H. Tenhunen, "Dark Silicon Patterning: Effi cient Power Utilization through Run-time Mapping", *in The Dark Side of Silicon (Computing in the Dark Silicon Era), Springer, 2016*.

Technical Report

TUCS T-R	**M.H. Haghbayan**, A.M. Rahmani, A.Y. Veldezion, J. Plosila, P. Liljeberg, A. Jantsch, and H. Tenhunen, "Adaptive Power Capping for Dark Silicon Many-Core Systems", *in TUCS Technical Reports 1149, TUCS, 2015*.

Served as the technical program committee (TPC)

36th Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium (DFT 2023)
35th Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium (DFT 2022)

Served as reviewer in

Asian Journal of Control.
ACM Transactions on Embedded Computing Systems.
IEEE Transaction on Computers (TC)
IEEE Transaction on CAD (TCAD)
Journal of Systems Architecture (JSA-Elsevier)
Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium (DFT)
Euromicro Conf. on Parallel, Distributed, Network-based Computing

Programming languages and tools

VHDL, Verilog, SystemC, C, C++, C#, Python, Matlab.
Modelisim, dc, cadence, FPGA synthesis tools, PIN instrumentation, Matlab-Simulink toolbox: Simscape (+multibody and fluids), Machine learning and deep learning, Optimization and statistics, automotive, signal processing, control, image processing.

Teaching and Mentorship

Teaching	Multi-processor Architecture, Fall 2018 (*University of Turku*) Autonomous Systems Architecture, Fall 2019 (*University of Turku*) Autonomous Systems Architecture, Fall 2020 (*University of Turku*) Autonomous Systems Architecture, Fall 2021 (*University of Turku*) Autonomous Systems Architecture, Spring 2023 (*University of Turku*)
Supervised PhD students	Sherif Mohamed (*University of Turku*) Jawad Yasin (*University of Turku*)
Current PhD students	Dufre Wu (*University of Turku*) Henri Sulo (*University of Turku*) Miika Kolu (*University of Turku*) Amir Ijaz (*University of Turku*) M-Reza Nakhkesh (*University of Turku*) Sajad Shahsavari (*University of Turku*) Anam Tahir (*University of Turku*) Masoomeh Karami (*University of Turku*)
Supervised master students	Husam Hreitanin, Tingxuan Liang, Jingxian Xu, M-Javad Ghalavand, Zufa Yu (*University of Turku*) Elmira Karimi (*University of Tehran*)
Supervised summer internship	Suvi Jokinen (University of Turku, summer 2022)
Instructor	Interface Circuits and Lab (*Jahad Daneshgahi of Sharif University*) Spring 2010. Computer Architecture, Compiler Design, and their Lab (*Payame Noor University*) Fall 2009. VHDL design, Assembly Language and their lab (*Shahid Rajaee University*), Fall 2008.
Teacher assistant	VHDL Lab, *University of Turku*, Fall 2013-2017. Digital Logic Design, *University of Tehran, School of ECE*, Fall 2010-2011. Robotics Lab, *University of Tehran*, School of ECE, Fall 2010-2011.

References

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